PLC -- Implementation of Traffic Light Controller

Purpose: To learn the use of the Allen Bradley PLC-5/20 with Sequential Function Charts (SFC) to implement a finite state machine which implements a traffic light controller.

Task 1: Implement a SFC system so that each time the normally-open momentary switch CLK is closed the system moves from the present state to the next state. CLK should be PT-8 SIM switch at I:000/00. The switch must be de-activated and re-activated before the system goes to the next state. The state diagram is shown in Figure 1. See table 1 for state definitions and table 2 for address assignments. You will find it useful to use the OSR (One-Shot Rising) instruction as part of the CLK transition. Verify your design is working by observing the SFC in the RSLogix design tool.

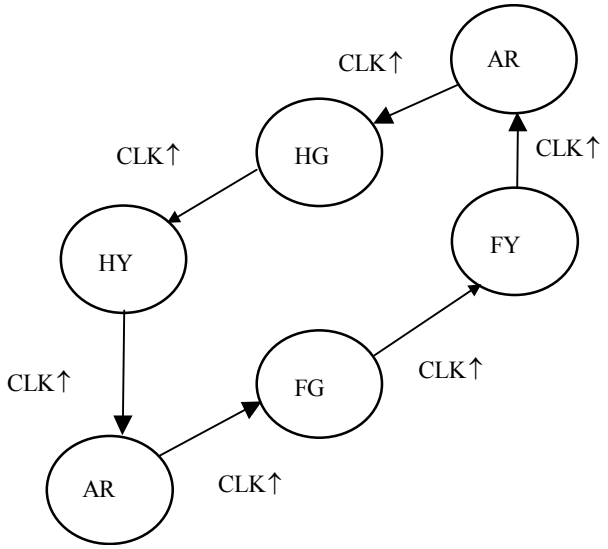


Figure 1 Initial Finite Sate Machine Sate Diagram

The state variables are HG (Highway Green), HY (Highway Yellow), AR (All Red), FG (Farmroad Green) and FY (Farmroad Yellow). The table 1 indicates the light condition for both the highway lights and farmroad lights

State	Highway Light	Frame Road Light
HG	Green	Red
HY	Yellow	Red
AR	Red	Red
FG	Red	Green
FY	Red	Yellow

Table 1 State and Light Assignments

Light	Address
Highway Red	O:003/0
Highway Yellow	O:003/1
Highway Green	O:003/2
Farm Road Red	O:003/3
Farm Road Yellow	O:003/4
Farm Road Green	O:003/5
Farm Road Loop North	O:003/6
Farm Road Loop South	O:003/7
Highway Loop East	O:003/10
Highway Loop West	O:003/11

Table 2 Light and Loop Address Assignments

Connect the Highway and Farmroad lights at a minimum using the address of table 2. Make sure MCP for A is assigned to the SFC file number. Otherwise the PLC-5/20 may not start in the proper file and the SFC might not function at all.

Task 2: Use a pair of traffic signal to simulate the intersection. One signal for the highway and one signal for the farm road. Use table 2 for your address assignments for your design. Use three of the timers in the PLC-5/20. One timer, called TS, is to provide a short delay of 2 second between; a second timer, called TM, is to provide a medium delay of 5 seconds, and a third timer, called TL, is to provide a long delay of 10 seconds. The timing is shown in Figure 2. These delays should replace the CLK signal. Place the timers in the action list files and the timer.DN bits in the transition files. Note when the transition is true the SFC does a post scan of the action list ladder, which resets the timer among other things. Figure 3 is the finite state diagram and should help in your design for the timed traffic light controller. Verify that your SFC is correct and then document your design.

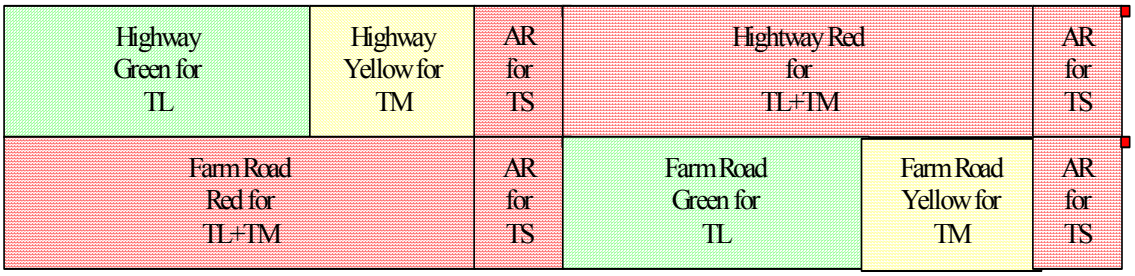


Figure 2 Traffic Light Timing (AR = All Red)

Task 3: Modify your implementation to match the requirement specification in the background section. Your implementation is to use two loops (both north and south sides of the intersection) in the farm road and two loops (both east and west side of the intersection) in the highway. These loops are called C in the background material. Use a counters/timer to give a delays of 5 seconds for the Short Time-out between green and red and a second counter/timer to give a delay of 10 seconds for the Long Time. Add additional timers if you need them. Before designing the SFC and ladder files draw a state diagram. Translate the state diagram to the SFC and then add the ladder files. . Verify that your SFC is correct and then document your design.

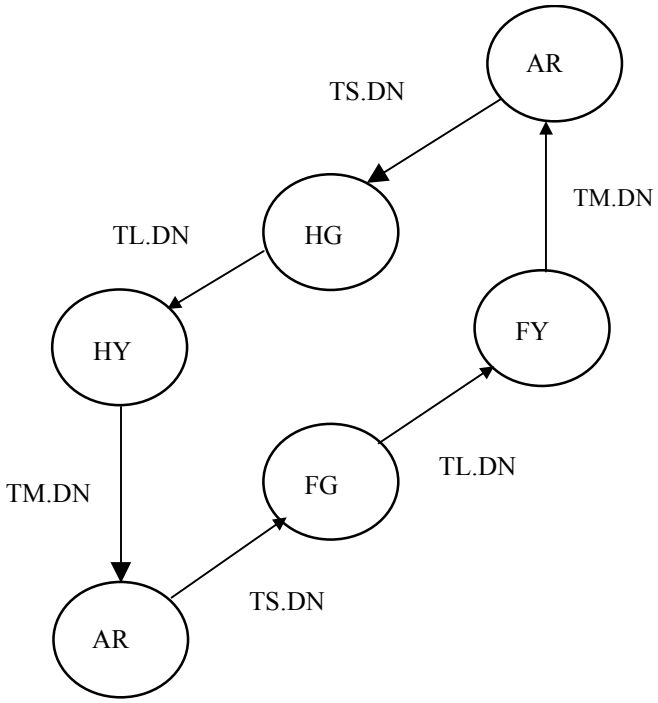
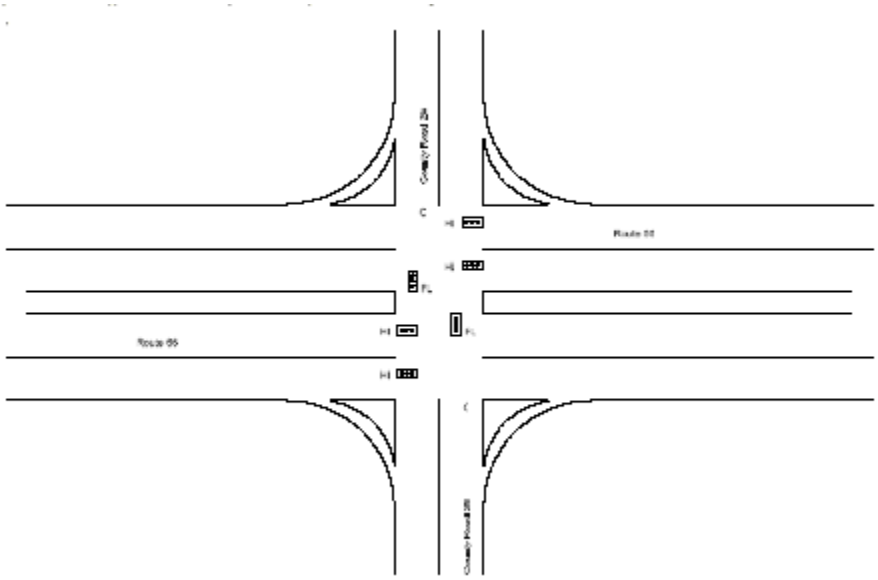


Figure 3 Timed Finite State Machine State Diagram

Task 4: Modify task 3 so that when the switch FLASH is closed the highway light flashes yellow and the farmroad light flashes red. The FLASH mode is ignored until the finite state machine is at the end of all red. The on time is 0.5 seconds and the off time is 0.5 seconds. The FLASH switch should be PT-8 SIM switch at I:000/00. When the FLASH switch is next opened, the finite state machine goes to highway green for 15 seconds and then proceeds to the normal highway yellow state. Draw a state diagram before implementing your design. Translate the state diagram to the SFC and then specify the ladder files. . Verify that your SFC is correct and then document your design.

Background: For your convenience the traffic light controller taken from Introduction to VLSI Systems by Carver Mead and Lynn Conway is presented here.

> *A busy highway is intersected by a little-used farmroad, as shown in figure4. Detectors are installed that cause signal C to go high in the presence of a car or cars on the farmroad at the position labeled C. We wish to control traffic lights at the intersection, so that in the absence of any cars waiting to cross or turn left on the highway from the farmroad, the highway lights will turn green. If any cars are detected at either position C, we wish the highway lights to cycle through caution to all red and the farmroad light then to turn green. The farmroad lights are to remain green only while the detectors signal the presence of a car or cars, but never longer than some fraction of a minute. The farmroad lights are then to cycle through caution to all red and the highway lights then turn to green. The highway lights are not to be interruptible again by the farmroad traffic until some fraction of a minute has passed.*



NOTE: The Master Control Program can be specified by selection MPC tab of the Processor Status. You may also want to set the SFC to reset on restart. This bit can be found under other tabs.

It is good design practice to keep timers out of the transition ladder. Place a single rung in the transition ladder that is terminated with an EOT instruction.

The traffic loop detectors have the following pin out. See the side of the Sarasota 215B/MS for tuning instructions. Energize unit for approximately 5 minutes before attempting to tune to allow device to stabilize.